Optimum Supply Voltage and Sleep Transistor Sizing
for Energy Minimization in Latency-Constrained MTCMOS Circuits

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Abstract—There have been extensive studies of voltage scaling in subthreshold circuits in order to minimize energy consumption. However, power consumption in stand-by mode and MTCMOS circuits have been overlooked. In this paper, energy consumption of subthreshold MTCMOS circuit is analyzed. Power supply and sleep transistor size are optimized to minimize energy consumption when a latency constraint is given. Energy consumption due to dynamic switching and leakage is considered in standby mode as well as in active mode. Simulation results in 65nm CMOS process show the dependence of energy consumption on supply voltage, sleep transistor size and the latency constraint.

I. INTRODUCTION

In order to reduce the energy consumption of digital integrated circuits, supply voltage scaling has been a widely used technique. For low performance applications such as sensors, voltage scaling has been pushed to the regime where circuits operate in the sub-threshold region [1]. Extensive studies have been performed to optimize various parameters for low energy operation in subthreshold circuits [2], [3]. In [2], optimum supply and threshold voltage is analytically derived and verified for minimum energy for a certain frequency of operation. Unfortunately, for a latency constrained application, the solution given in [2] alone does not result in minimum energy, since it considers energy consumption only during the active mode when a specific operating frequency is given. To achieve minimum energy consumption for a latency constrained circuit, one must also choose the optimum frequency of operation and consider the energy consumption during the standby mode as well.

In this paper, optimum supply voltage and operating frequency is analyzed for a latency constrained circuit. We assume that the latency is long enough such that the minimum energy is achieved when the circuit operates in the subthreshold region. As opposed to previous works which only consider low-Vth subthreshold circuits in active mode [4], we propose subthreshold MTCMOS circuits that reduces leakage current in active mode as well as in stand-by mode. In addition, by analyzing the trade-off between the dynamic and leakage energy in the active and stand-by modes, various parameters are optimized for minimum energy, including supply voltage, sleep transistor size, and the duration of active and standby modes for a given certain latency.

II. MINIMIZING ENERGY CONSUMPTION IN A LATENCY-CONSTRAINED CIRCUIT

A. MTCMOS in subthreshold region

Scenarios for different energy consumption in a latency constrained circuit are illustrated in Fig. 1 (a) and (b), where identical circuits perform the same function for a given workload with the differences being their clock frequency and \( V_{DD} \). As can be seen, a high-\( V_{DD} \) circuit allows faster operation and hence has shorter active time than a low-\( V_{DD} \) circuit, while the opposite is true for standby time. Since the low-\( V_{DD} \) circuit has longer active mode and hence shorter standby mode, the energy consumption due to standby leakage and dynamic switching is smaller than that of the high-\( V_{DD} \) circuit. However, the energy consumption due to leakage in active mode can be larger due to increased active time, especially in deep submicron CMOS processes, despite the lower \( V_{DD} \). Hence there exists a trade-off between the energy consumption from active leakage and energy consumption from standby leakage and dynamic switching. Although previous work have exploited this trade-off and provided optimum \( V_{DD} \) and \( V_{th} \) for minimum energy, standby leakage was ignored. In addi-
IV. Energy consumption of MTCMOS circuit in subthreshold
region

A simple MTCMOS circuit on the other hand can easily reduce the leakage current. For simplicity, consider two inverter circuits operating in subthreshold region as shown in Fig. 2. When the sleep transistor in Fig. 2 (a) is turned on, note that it is in a weaker subthreshold region than the low-\(V_{th}\) devices due to its higher \(V_{th}\). Hence, the current in the active mode, which includes the leakage, is smaller than that of the conventional inverter shown in Fig 2(b).

Also note that when the sleep transistor is turned off, the leakage current is significantly reduced compared to that of the conventional inverter. Therefore, MTCMOS circuit in subthreshold region can provide large energy savings. This is verified in Table 1, which shows the simulation results of two 9-stage ring oscillators that are identical except for the sleep transistor. In order to make a fair comparison, supply voltage is adjusted such that not only their frequency but also their voltage swing is the same. It can be seen that the MTCMOS circuit has the much smaller standby leakage power\(^1\).

B. Energy consumption of MTCMOS circuit in subthreshold region

The energy consumption \(E_T\) of an MTCMOS circuit is simply the sum of dynamic switching energy \(E_{DY N}\) and the leakage energy during active \(E_{L\_AC}\) and standby modes \(E_{L\_ST}\), as described by the following equation.

\[
E_T = E_{DY N} + E_{L\_AC} + E_{L\_ST}
\]

\(^1\)Standby leakage power is measured by cutting the ring oscillator loop

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>COMPARISON OF MTCMOS AND CONVENTIONAL RING OSCILLATORS IN SUBTHRESHOLD REGION.</th>
</tr>
</thead>
<tbody>
<tr>
<td>frequency</td>
<td>170.4MHz</td>
</tr>
<tr>
<td>(V_{DD})</td>
<td>0.295V</td>
</tr>
<tr>
<td>(V_{Swing})</td>
<td>0.295V</td>
</tr>
<tr>
<td>Active power</td>
<td>0.80nW</td>
</tr>
<tr>
<td>Standby power</td>
<td>25.63nW</td>
</tr>
</tbody>
</table>

Each component in the righthand side of the above equation can be represented by the following equations,

\[
E_{DY N} = C_{eff}V_{DD}^2
\]

\[
E_{L\_AC} = V_{DD}I_{L\_AC}T_{active}
\]

\[
E_{L\_ST} = V_{DD}I_{L\_ST}T_{stry}
\]

where \(C_{eff}\) is the total capacitance that is charged to perform the desired function for a given workload, \(V_{DD}\) is the supply voltage, \(T_{active}\) and \(T_{stry}\) are the time duration of the circuit in active and standby modes, respectively.

Unlike the MTCMOS circuit in strong inversion, the leakage currents \(I_{L\_AC}, I_{L\_ST}\) in Eq. 3 and 4 deserve special attention, since the sleep transistor is not fully turned on in active mode but stays in weaker subthreshold region than the low-\(V_{th}\) devices. Therefore, currents in active mode is not only determined by the low-\(V_{th}\) devices but it is also heavily governed by the high-\(V_{th}\) sleep transistor as well. Note that if the sleep transistor is large enough such that the current in active mode is not affected by the sleep transistor, the stand-by leakage currents can be determined by the low-\(V_{th}\) devices and sleep transistor will be unable to reduce the standby leakage current. Hence, careful sizing of MTCMOS is necessary in the subthreshold region.

Based on the above analysis, the leakage currents in active and standby modes \(I_{L\_AC}, I_{L\_ST}\) can be described as,

\[
I_{L\_AC} = \alpha_1I_{eff}e^{-\frac{V_{th1}}{nV_{T}}} (1 - e^{-\frac{V_{th1}}{nV_{T}}} + \alpha_2I_{sleep}e^{-\frac{V_{th2}}{nV_{T}}} (1 - e^{-\frac{V_{th2}}{nV_{T}}} \text{ (5)}
\]

\[
I_{L\_ST} = W_{sleep}I_{o}e^{-\frac{V_{th1}}{nV_{T}}} (1 - e^{-\frac{V_{DD}}{nV_{T}}} \text{ (6)}
\]

where \(W_{eff}\) is the effective total width of transistors that contributes to leakage energy during the active mode, \(W_{sleep}\) is the width of the sleep transistor, \(V_{th1}\) and \(V_{th2}\) are the threshold voltage of low-\(V_{th}\) and high-\(V_{th}\) transistors, respectively. It is assumed that the leakage current in standby mode is completely determined by the sleep transistor while the leakage current in active mode is governed by both low-\(V_{th}\) and high-\(V_{th}\) transistors with weighting factors \(\alpha_1\) and \(\alpha_2\).

In Eq. 5, \(V_{DS2}\) is the virtual ground in MTCMOS circuits, and the virtual ground voltage increases as the size of sleep transistor is reduced.

The active time \(T_{active}\) and standby time \(T_{stry}\) of Eq. 3 and 4 can be represented as the below equations,

\[
T_{active} = \frac{K_{1}C_{eff}V_{DD}}{I_{active}} = K_{2}T_{delay}
\]

\[
T_{stry} = T_{latency} = T_{active}
\]

\(^2\)\(\alpha_1\) and \(\alpha_2\) are not constants but are functions of various parameters used in the subthreshold equation. When \(W_{sleep}\) is much shorter than \(W_{eff}\), currents in active mode is heavily governed by the high-\(V_{th}\) sleep transistor. Therefore, \(\alpha_1\) becomes close to 0 and \(\alpha_2\) close to 1. On the other hand, if the sleep transistor is large enough such that the current in active mode is not affected by the sleep transistor, \(\alpha_1\) goes to 1 and \(\alpha_2\) goes to 0.
where \( I_{\text{active}} \) is the average current that charges or discharges the effective load capacitor \( C_{\text{eff}} \) in active mode, \( T_{\text{delay}} \) is the propagation delay of the circuit and \( K_1, K_2 \) are a fitting parameter. As previously mentioned, note that \( I_{\text{active}} \) is affected by the \( W_{\text{sleep}} \) of the sleep transistor. This can be seen in the simulation results of Fig. 3 which shows the delay of an MTCMOS circuit vs. \( W_{\text{sleep}} \), for different values of \( V_{DD} \). It can be seen that the impact of \( W_{\text{sleep}} \) on delay is greater when \( V_{DD} \) is smaller, when the current is smaller.

Substituting Eq. 2-7 in Eq. 1 allows us to get a detailed expression for total energy consumption for a given latency, where optimum values of \( V_{DD} \) and \( W_{\text{sleep}} \) can be found. Once these values are found, other parameters such as the optimum duration of active and standby mode, follow from Eq. 7 and 8.

III. SIMULATION RESULTS: OPTIMUM \( V_{DD} \) AND SLEEP TRANSISTOR SIZE FOR MTCMOS CIRCUIT IN SUBTHRESHOLD REGION

Although the analytical equations have been provided in the previous section, the equations that involve leakage currents are not straightforward and hence requires complex computation. In this section, simulation results of a digital circuit with 7500 transistors, are shown. Parameters for 65nm CMOS BPTM model are used in the simulation. In order to find the optimum supply and sleep transistor size, the following simulations show results when two of the three variables (\( V_{DD}, W_{\text{sleep}}, \) and \( T_{\text{latency}} \)), are changed while the other variable is kept constant.

A. Optimum \( V_{DD} \) with respect to latency constraint

In this section, we analyze the optimum \( V_{DD} \) as latency constraint is varied, with a fixed sleep transistor size. The profile of energy consumption is shown in Fig. 4 and 5, where the contribution of energy consumption from dynamic switching \( (E_{\text{dyn}}) \) active \( (E_{L,AC}) \) and standby leakage \( (E_{L,ST}) \) are shown. In Fig. 4, leakage energy in active mode is reduced as \( V_{DD} \) is increased. This is because the circuit operates at a high enough frequency such that the time spent in active mode is further reduced than the increase in leakage current. The leakage energy in standby mode increases with \( V_{DD} \), since time spent in standby mode increases. Similar trend is also seen in Fig. 5 which has larger latency of \( T_{\text{latency}} = 100\mu s \). As latency is increased, the impact due to standby leakage becomes significant and hence the optimum \( V_{DD} \) is reduced.

B. Optimum sleep transistor size with respect to latency constraint

The optimum sleep transistor size with respect to different latency constraint is shown in Fig. 6 and 7, with the \( V_{DD} \) fixed. Similar to the analysis shown in previous sections, the optimum size of the sleep transistor results from the trade-off between active and standby energy consumption. It can be seen that the optimum value of sleep transistor is reduced as the required latency is increased.

When the required latency is short, as shown in Fig. 6, circuits spend almost all of their time in active mode. Hence, \( W_{\text{sleep}} \) should be sized such that circuit can operate faster and spend more time in standby mode. On the other hand, when the
as well as in standby mode. The supply voltage and the size of MTCMOS is used to reduce the leakage current in active mode. It has been analyzed. In order to improve the energy efficiency, the optimum $W/L$ portion of the overall power and $V_{DD}$ spend most of the time in active mode. However, as latency increases, $W/L$ of sleep transistor is critical to achieve low energy operation. It is seen that low-$V_{DD}$ is preferred for large latency and vice versa for small latency. Although similar result is seen for the sleep transistor, the effect of $W_{sleep}$ becomes increasingly more important as the latency is increased.

V. ACKNOWLEDGMENT

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REFERENCES