A Low-Jitter Area-Efficient LC-VCO Based Clock Generator in 0.13-µm CMOS

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SUMMARY This letter presents an ultra low-jitter clock generator that employs an area-efficient LC-VCO. In order to fully utilize the area of the on-chip inductor, the loop filter of a phase locked loop (PLL) is located underneath the inductor. A prototype chip implemented in 0.13-µm CMOS process achieves 105 MHz to 225 MHz of clock frequency while consuming 4.2 mW from 1.2 V supply. The measured rms jitter and normalized rms jitter of the proposed clock generator are 2.8 ps and 0.031% at 105 MHz, respectively.

key words: clock generator, LC-VCO, area-efficient LC-VCO

1. Introduction

As the need for high performance systems is increased in modern VLSI designs, accuracy of clock becomes an important issue. In the area of clock generators, ring VCOs have been widely used due to their small area and wide frequency range. However, they are not suitable for ultra low-jitter clock generators because of their limitation in minimum achievable jitter [1]. Hence, for applications that require ultra low-jitter of less than 0.1%, LC-VCOs have been used despite their large area [2], [3].

Recently, there have been some investigations on how the area of the on-chip inductor can be better utilized [4], [5]. In [4], the RF characteristics of a MOSFET and an inductor are characterized when they are placed together. In [5], an LC-VCO with its cross-coupled $-g_m$ transistors and varactors underneath the inductor has been demonstrated. However, the area of the inductor was not fully utilized due to the small size of the active circuits. In addition, the operation of the LC-VCO was not demonstrated in a phase locked loop (PLL).

In this letter, a 105 MHz to 225 MHz ultra low-jitter clock generator is proposed which employs an LC-VCO and a 3rd order loop filter located underneath the inductor, thereby improving the jitter performance and the area efficiency. The proposed clock generator is the first PLL to demonstrate that it is possible to fully integrate the passive loop filter under the inductor.

2. Architecture

It is difficult to use the LC-VCO as low jitter clock at a few hundred MHz due to the low quality factor of the inductor. Hence, in order to generate a low jitter clock, an LC-VCO with a multi-modulus frequency divider is used as shown in Fig. 1. By taking the output of the first frequency divider, a low jitter clock can be achieved in the desired frequency range of 105 MHz to 225 MHz. Note that the output jitter is dominated by the VCO and the dividers add little noise to the output jitter. Taking the output from the first divider has another advantage that the variation of the loop bandwidth is reduced [3].

Because the phase noise of the PLL can be degraded due to the high VCO gain, the division values of frequency dividers are chosen to minimize the tuning range of the LC-VCO for the low VCO gain. The M divider has division values of 12, 14, 16, 18, 20 and 22, which ensures the 50% duty cycle of the output clock due to even numbers of the division values. In the N divider, the division values is from 3 to 8 and the step of the division values is 0.5.

3. Area-Efficient LC-VCO

The schematic of the area-efficient LC-VCO is shown in Fig. 2(a). A tail current source which is one of the major contributors to the phase noise is removed to improve the phase noise. To minimize the effects of common mode noise from digital circuits, a differentially controlled scheme is employed in the LC-VCO with a tuning range of 2.08 GHz to 2.45 GHz. The schematic of the 3rd order loop filter is
shown in Fig. 2(b). The MOS capacitors (MOSCAPs) are used instead of the Metal-insulator-Metal (MiM) capacitor to reduce the area of the loop filter. The source and drain of the MOSCAPs are connected to the supply voltage to always turn on the MOSCAPs, which guarantees the constant capacitance of the MOSCAPs.

In order to fully utilize the area of the inductor, the loop filter whose area is 0.033 mm$^2$ is located underneath the inductor as shown in Fig. 3(a) instead of the cross-coupled $g_m$ transistors and varactors that occupy 0.009 mm$^2$. However, placing the MOSCAPs and resistors underneath the inductor increases the parasitic capacitance of the inductor and reduces the quality factor. To reduce the parasitic capacitance, only metal 1 is used in laying out the MOSCAPs of the loop filter. In addition, multiple small MOSCAPs are used instead of large MOSCAPs, which act as a patterned ground shield (PGS) and reduce the eddy current loops, hence improving the quality factor. Moreover, MOSCAPs are not placed directly under the center of the inductor to reduce the degradation of the quality factor since the magnetic field is the strongest at the center.

The quality factor of the inductors using a 3D-electromagnetic (EM) simulator is shown in Fig. 3(b) for three cases: a standard inductor without MOSCAP arrays underneath and inductors with 9 µm × 9 µm and 15 µm × 15 µm unit MOSCAP arrays underneath. The quality factor of the standard 3.3 nH inductor is about 15 at 2.2 GHz. It can be seen that when 15 µm × 15 µm MOSCAPs are underneath the inductor, the quality factor is degraded to 11. However, when 9 µm × 9 µm MOSCAPs are used, the degradation is small as the MOSCAPs act as the PGS.

4. Measurement Results

The die photo of the clock generator and a conventional LC-VCO implemented in a 0.13 µm CMOS process is shown in Fig. 4. The conventional LC-VCO which uses a standard inductor is also implemented for performance comparison with the area-efficient LC-VCO. The core size of the clock generator and the conventional LC-VCO is 0.07 mm$^2$ and 0.1 mm$^2$, respectively, excluding pads. The standard inductor used in the conventional LC-VCO and provided by the foundry has a dummy layer to define an inductor region. Hence, the distance between the inductor and the dummy layer is larger than 50 µm. Moreover, the width of the dummy layer including three lines of 3 × 3 µm$^2$ dummy metal islands with 3 µm spacing is larger than 18 µm and active devices and passive devices are not allowed inside the dummy region. In order to place MOSCAPs under the inductor for improving area efficiency, we re-designed the inductor by removing the dummy layer and using the 3D-EM simulator. Therefore, the modified inductor with MOSCAP arrays underneath is smaller than the standard inductor as shown in Fig. 4.

The measured phase noise of two LC-VCOs at 2.422 GHz is shown in Fig. 5. It can be seen that there is about 2 dB difference between the two plots due to the
degradation of the quality factor. The phase noise of the frequency divider at 105 MHz is shown in Fig. 6 and the measured rms jitter integrated over 1 kHz to 40 MHz is 2.97 ps (0.031%). The performance of the clock generator is summarized in Table 1 together with other low-jitter clock generators. It can be seen that the normalized jitter of the proposed clock generator is smaller than other clock generators. Moreover, it can be seen that the proposed clock generator has the smallest area and power consumption although it uses the LC-VCO.

5. Conclusions

In this letter, an ultra low-jitter PLL-based clock generator that employs an area-efficient LC-VCO is presented for the first time. In order to improve the area efficiency, MOS capacitors and resistors of the loop filter are located underneath the on-chip inductor. The measured normalized rms jitter of the proposed clock generator is less than 0.065% over the frequency range of 105 MHz to 225 MHz.

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References